II. Listing of Claims

1. (Currently Amended): An integrated field-effect transistor, having a substrate region surrounded:

by two terminal regions, one terminal region being a source region and the other terminal region being a drain region,

by two electrically insulating insulating layers, which are arranged at mutually opposite sides of the substrate region and are adjoined by control regions, by two electrically insulating regions, the insulating regions being arranged at mutually opposite sides of the substrate region, and

by an electrically conductive connecting region or a part of an electrically conductive connecting region which produces an electrically conductive connection between one of the terminal regions and the substrate region, the connecting region comprising a metal-semiconductor compound,

part of a covering area of the substrate region being covered by the connecting region, ~~which extends further over~~ the connecting region also covering a covering area of the source region, the part of the covering area of the substrate region covering the substrate region between the insulating layers and between the control regions.

2. (Original): The field-effect transistor as claimed in claim 1, wherein the conductive connecting region comprises at least one of: a silicide of a metal having a melting point of greater than 1400 degrees Celsius, a refractory metal silicide or a rare earth metal silicide.

3. (Original): The field-effect transistor as claimed in claim 1, wherein at least one of:

the insulating layers for insulating the control regions from the substrate region have an insulation strength of at least fifteen nanometers,

a distance between the terminal regions is at least 0.3 micrometer, and

one terminal region or both terminal regions have a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than five volts.

4. (Original): The field-effect transistor as claimed claim 1, wherein at least one of:

one insulating region is part of an insulating layer which carries a multiplicity of field-effect transistors,

the insulating layer comprises silicon dioxide, and

the other insulating region is part of an insulating layer, which insulates a multiplicity of substrate regions.

5. (Currently Amended): The field-effect transistor as claimed in claim 1,

wherein the substrate region at least one of:

contains a monocrystalline semiconductor material; and

is doped in accordance with one conduction type[[,]] and ~~wherein~~ the terminal regions are doped in accordance with ~~the other~~ another conduction type.

6. (Original): The field-effect transistor as claimed in claim 1, wherein the control regions are electrically conductively connected to one another.

7. (Original): The field-effect transistor as claimed in claim 1, wherein at least one of:

the substrate region contains six side areas,

the terminal regions are arranged at mutually opposite sides of the substrate region, and

the control regions are arranged at mutually opposite sides of the substrate region.

8. (Original): The field-effect transistor as claimed in claim 1, wherein switching voltages having a magnitude of greater than nine volts are able to be switched by the field-effect transistor.

9. (Original): The field-effect transistor as claimed in claim 1, the field-effect transistor being a driving transistor on a word line or a bit line of a memory cell array, the driving transistor applying a control voltage to the word line or to the bit line.

10. (Withdrawn): A method for fabricating a field-effect transistor the method comprising the following steps without restriction by the order specified:

forming a substrate region,

forming two terminal regions at the substrate region, one terminal region being a source region and the other terminal region being a drain region,

forming two electrically insulating insulating layers, which are arranged at mutually opposite sides of the substrate region and are adjoined by control regions,

forming an electrically conductive connecting region, which electrically conductively connects one of the terminal regions and the substrate region the conductive connecting region comprising a metal-semiconductor compound,

leveling a surface by chemical mechanical polishing after forming the control regions,

etching-back the control regions after polishing, and

performing a self-aligning method for forming the metal-semiconductor compound in the etched-back regions, on the substrate region, and on a terminal region.

11. (Withdrawn): The method as claimed in claim 10, wherein at least one of:

at least one of the terminal regions or the substrate region comprises silicon,

the connecting region comprises silicide,

the connecting region is produced by means of a self-aligning method in which a metal is deposited, which forms the metal-semiconductor compound at semiconductor regions, and the metal is removed in regions in which the metal-semiconductor compound was formed.

12. (Withdrawn): The method as claimed in claim 10 further comprising at least one of:

providing an SOI substrate,

patterning the silicon of the SOI substrate, regions remaining in which the substrate region and the terminal regions are intended to be arranged,

forming the control region after the patterning, and

filling of free regions between the regions that remain with an electrically insulating material.

13. (Withdrawn): The method as claimed in claim 12, further comprising leveling a surface at least one of after the filling and after forming the control regions.

14. (Withdrawn): The method as claimed in claim 13, further comprising performing a self-aligning salicide method for forming the metal-semiconductor compound.

15. (New): The method as claimed in claim 1, wherein the substrate region is p-doped.

16. (New): The method as claimed in claim 1, wherein the substrate region is n-doped, thereby producing a p-channel enhancement mode transistor.

III Amendments to Drawings

A replacement sheet of drawings including changes to Figure 1 is attached.